What Is Claimed Is:

1. An electrically programmable and erasable memory device, comprising:

a substrate of semiconductor material having a first conductivity type and a surface;

a pair of trenches formed into the substrate surface, wherein a strip of the substrate is disposed between the pair of trenches;

a first region of a second conductivity type formed in the substrate strip;

a pair of second regions of the second conductivity type formed in the substrate and spaced apart from the first region;

a pair of channel regions each extending from the first region to one of the second regions and each having a first portion extending underneath one of the trenches, a second portion not disposed in the substrate strip and extending along the one trench, and a third portion extending along the substrate surface;

a pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the trenches; and

a pair of electrically conductive control gates each disposed over and insulated from one of the channel region third portions.

2. The device of claim 1, wherein each of the floating gates is disposed adjacent to and insulated from the first and second portions of one of the channel regions for controlling a conductivity thereof.

3. The device of claim 1, wherein each of the channel regions includes a fourth portion disposed in the substrate strip and extending along one of the trenches.

4. The device of claim 3, wherein each of the floating gates is disposed adjacent to and insulated from the first, second and fourth portions of one of the channel regions for controlling a conductivity thereof.

5. The device of claim 3, wherein the channel region first and third portions are generally parallel to the substrate surface, and the channel region second and fourth portions are generally perpendicular to the substrate surface.

6. The device of claim 3, wherein the floating gates extend deeper into the substrate than does the first region.

7. The device of claim 1, wherein:

each of the trenches includes opposing first and second sidewalls and a bottom wall;

the first region is disposed between the first sidewalls of the pair of trenches;

each of the channel region first portions is disposed along one of the bottom walls; and

each of the channel region second portions is disposed along one of the second sidewalls.

8. The device of claim 3, wherein:

each of the trenches includes opposing first and second sidewalls and a bottom wall;

the first region is disposed between the first sidewalls of the pair of trenches;

each of the channel region fourth portions is disposed along one of the first sidewalls;

each of the channel region first portions is disposed along one of the bottom walls; and

each of the channel region second portions is disposed along one of the second sidewalls.

9. The device of claim 1, wherein each of the floating gates has an edge that faces one of the control gates and is insulated therefrom with insulation material having a thickness that permits tunneling of charges from the edge to the one control gate.

10. The device of claim 1, wherein the first region is disposed laterally adjacent to and insulated from the floating gates.

11. The device of claim 1, further comprising:

an electrically conductive erase gate that is insulated from the floating gates and the control gates, wherein each of the floating gates has an edge that faces the erase gate and is insulated therefrom with insulation material having a thickness that permits tunneling of charges from the edge to the erase gate.

12. The device of claim 1, further comprising:

a second pair of trenches formed into the substrate surface, wherein a second strip of the substrate is disposed between the second pair of trenches, and wherein one of the second regions is formed in the second substrate strip;

one of the channel regions includes a fourth portion not disposed in the second substrate strip and extending along one of the second pair of trenches, and a fifth portion extending underneath one of the second pair of trenches; and

a second pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the second pair of trenches.

13. The device of claim 12, wherein the control gates are integrally formed together from continuously formed conductive material.

14. The device of claim 3, further comprising:

a second pair of trenches formed into the substrate surface, wherein a second strip of the substrate is disposed between the second pair of trenches, and wherein one of the second regions is formed in the second substrate strip;

one of the channel regions includes a fifth portion not disposed in the second substrate strip and extending along one of the second pair of trenches, a sixth portion extending underneath one of the second pair of trenches, and a seventh portion disposed in the second substrate strip and extending along one of the second pair of trenches; and

a second pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the second pair of trenches.

15. An array of electrically programmable and erasable memory devices, comprising:

a substrate of semiconductor material having a first conductivity type and a surface;

spaced apart isolation regions of the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a plurality of pairs of memory cells, wherein each of the memory cell pairs comprises:

a pair of trenches formed into the substrate surface, wherein a strip of the substrate is disposed between the pair of trenches,

a first region of a second conductivity type formed in the substrate strip,

a pair of second regions of the second conductivity type formed in the substrate and spaced apart from the first region,

a pair of channel regions each extending from the first region to one of the second regions and each having a first portion extending underneath one of the trenches, a second portion not disposed in the substrate strip and extending along the one trench, and a third portion extending along the substrate surface,

a pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the trenches, and

a pair of electrically conductive control gates each disposed over and insulated from one of the channel region third portions.

16. The array of claim 15, wherein each of the floating gates is disposed adjacent to and insulated from the first and second portions of one of the channel regions for controlling a conductivity thereof.

17. The array of claim 15, wherein each of the channel regions includes a fourth portion disposed in one of the substrate strips and extending along one of the trenches.

18. The array of claim 17, wherein each of the floating gates is disposed adjacent to and insulated from the first, second and fourth portions of one of the channel regions for controlling a conductivity thereof.

19. The array of claim 17, wherein the channel region first and third portions are generally parallel to the substrate surface, and the channel region second and fourth portions are generally perpendicular to the substrate surface.

20. The array of claim 17, wherein the floating gates extend deeper into the substrate than do the first regions.

21. The array of claim 15, wherein:

each of the trenches includes opposing first and second sidewalls and a bottom wall;

each of the first regions is disposed between the first sidewalls of one of the trench pairs;

each of the channel region first portions is disposed along one of the bottom walls; and

each of the channel region second portions is disposed along one of the second sidewalls.

22. The array of claim 17, wherein:

each of the trenches includes opposing first and second sidewalls and a bottom wall;

each of the first regions is disposed between the first sidewalls of one of the trench pairs;

each of the channel region fourth portions is disposed along one of the first sidewalls;

each of the channel region first portions is disposed along one of the bottom walls; and

each of the channel region second portions is disposed along one of the second sidewalls.

23. The array of claim 15, wherein each of the floating gates has an edge that faces one of the control gates and is insulated therefrom with insulation material having a thickness that permits tunneling of charges from the edge to the one control gate.

24. The array of claim 15, wherein each of the first regions is disposed laterally adjacent to and insulated from one of the floating gate pairs.

25. The array of claim 15, further comprising:

a plurality of conductive control lines of conductive material each extending across the active and isolation regions in a second direction perpendicular to the first direction and each electrically connecting together one of the control gates from each of the active regions.

26. The array of claim 15, further comprising:

a plurality of conductive source lines of conductive material each extending across the active and isolation regions in a second direction perpendicular to the first direction and each electrically connecting together one of the first regions from each of the active regions.

27. The array of claim 15, wherein each of the memory cell pairs further comprises:

an electrically conductive erase gate that is insulated from the pair of floating gates and the pair of control gates, wherein each of the floating gates has an edge that faces the erase gate and is insulated therefrom with insulation material having a thickness that permits tunneling of charges from the edge to the erase gate.

28. The array of claim 27, further comprising:

a plurality of conductive erase lines of conductive material each extending across the active and isolation regions in a second direction perpendicular to the first direction and each electrically connecting together one of the erase gates from each of the active regions.

29. An array of electrically programmable and erasable memory devices, comprising:

a substrate of semiconductor material having a first conductivity type and a surface;

spaced apart isolation regions of the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a plurality of pairs of memory cells, wherein each one of the memory cell pairs comprises:

a pair of trenches formed into the substrate surface, wherein a strip of the substrate is disposed between the pair of trenches,

a first region of a second conductivity type formed in the substrate strip,

a pair of channel regions each extending from the first region of the one pair of memory cells to first regions of adjacent pairs of memory cells, wherein each of the channel regions includes a first portion extending underneath one of the trenches, a second portion not disposed in the substrate strip and extending along the one trench, a third portion extending along the substrate surface, a fourth portion extending along one of the trenches for one of the adjacent pairs of memory cells and a fifth portion extending underneath the one trench from the one adjacent pair of memory cells,

a pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the trenches, and

a pair of electrically conductive control gates each disposed over and insulated from one of the channel region third portions.

30. The array of claim 29, wherein for each of the active regions, the control gates therein are integrally formed together from continuously formed conductive material.

31. The array of claim 29, wherein each of the channel regions further includes:

a sixth portion disposed in the substrate strip for the one memory cell pair and extending along one of the trenches for the one memory cell pair; and

a seventh portion disposed in the substrate strip for the one adjacent pair of memory cells and extending along one of the trenches for the one adjacent pair of memory cells.

32. A method of forming a semiconductor memory cell, comprising:

forming a pair of trenches into a surface of a semiconductor substrate of a first conductivity type, wherein a strip of the substrate is disposed between the pair of trenches;

forming a first region of a second conductivity type in the substrate strip;

forming a pair of second regions of the second conductivity type in the substrate and spaced apart from the first region, wherein a pair of channel regions each extend from the first region to one of the second regions and each have a first portion extending underneath one of the trenches, a second portion not disposed in the substrate strip and extending along the one trench, and a third portion extending along the substrate surface;

forming a pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the trenches; and

forming a pair of electrically conductive control gates each disposed over and insulated from one of the channel region third portions.

33. The method of claim 32, wherein the formation of the pair of trenches includes:

forming material over the substrate;

forming a first trench in the material that extends down to and exposes the substrate;

forming a mask material in the first trench and over a center portion of the exposed substrate; and

performing an etch that forms the pair of trenches into the exposed portion of the substrate on either side of the mask material, wherein the mask material is disposed over the strip of the substrate.

34. The method of claim 32, wherein the formation of the mask material includes:

forming opposing spacers in the first trench, wherein the center portion of the exposed substrate is left exposed therebetween; and

forming the mask material on the substrate exposed center portion by thermal oxidation.

35. The method of claim 32, further comprising:

extending the second trench into the substrate before the formation of the pair of trenches.

36. The method of claim 32, further comprising:

forming edges on the floating gates; and

forming a conductive erase gate that is insulated from the floating gates and the control gates, wherein the floating gate edges face the erase gate and are insulated therefrom with insulation material having a thickness that permits tunneling of charges from the edges to the erase gate.

37. The method of claim 32, wherein each of the floating gates is formed adjacent to and insulated from the first and second portions of one of the channel regions for controlling a conductivity thereof.

38. The method of claim 32, wherein each of the channel regions further includes a fourth portion disposed in the substrate strip and extending along one of the trenches.

39. The method of claim 38, wherein each of the floating gates is formed adjacent to and insulated from the first, second and fourth portions of one of the channel regions for controlling a conductivity thereof.

40. The method of claim 38, wherein the channel region first and third portions are generally parallel to the substrate surface, and the channel region second and fourth portions are generally perpendicular to the substrate surface.

41. The method of claim 38, wherein the floating gates extend deeper into the substrate than does the first region.

42. The method of claim 35, wherein:

each of the trenches is formed to include opposing first and second sidewalls and a bottom wall;

the first region is disposed between the first sidewalls of the pair of trenches;

each of the channel region first portions is disposed along one of the bottom walls; and

each of the channel region second portions is disposed along one of the second sidewalls.

43. The method of claim 38, wherein:

each of the trenches is formed to include opposing first and second sidewalls and a bottom wall;

the first region is disposed between the first sidewalls of the pair of trenches;

each of the channel region fourth portions is disposed along one of the first sidewalls;

each of the channel region first portions is disposed along one of the bottom walls; and

each of the channel region second portions is disposed along one of the second sidewalls.

44. The method of claim 35, wherein each of the floating gates has an edge that faces one of the control gates and is insulated therefrom with insulation material having a thickness that permits tunneling of charges from the edge to the one control gate.

45. The method of claim 35, wherein the first region is disposed laterally adjacent to and insulated from the floating gates.

46. The method of claim 35, further comprising:

forming an electrically conductive erase gate that is insulated from the floating gates and the control gates; and

forming an edge on each of the floating gates that faces the erase gate and is insulated therefrom with insulation material having a thickness that permits tunneling of charges from the edge to the erase gate.

47. The method of claim 35, further comprising:

forming a second pair of trenches into the substrate surface, wherein a second strip of the substrate is disposed between the second pair of trenches, and wherein one of the second regions is formed in the second substrate strip;

wherein one of the channel regions includes a fourth portion not disposed in the second substrate strip and extending along one of the second pair of trenches, and a fifth portion extending underneath one of the second pair of trenches; and

forming a second pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the second pair of trenches.

48. The method of claim 47, wherein the control gates are integrally formed together from continuously formed conductive material.

49. The method of claim 38, further comprising:

forming a second pair of trenches into the substrate surface, wherein a second strip of the substrate is disposed between the second pair of trenches, and wherein one of the second regions is formed in the second substrate strip;

wherein one of the channel regions includes a fifth portion not disposed in the second substrate strip and extending along one of the second pair of trenches, a sixth portion extending underneath one of the second pair of trenches, and a seventh portion disposed in the second substrate strip and extending along one of the second pair of trenches; and

forming a second pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the second pair of trenches.

50. An electrically programmable and erasable memory device, comprising:

a substrate of semiconductor material having a first conductivity type and a surface;

a first trench formed into the substrate surface;

a second trench formed into the substrate surface that is spaced apart from the first trench by a portion of the substrate;

a first region of a second conductivity type formed in the substrate adjacent the first trench and not in the substrate portion;

a second region of the second conductivity type formed in the substrate adjacent the second trench and not in the substrate portion;

a channel region of the substrate extending between the first and second regions, wherein the channel region includes a first portion extending from the first region and along the first trench, a second portion extending underneath the first trench, a third portion disposed in the substrate portion and extending along the first trench, a fourth portion disposed in the substrate portion and extending along the substrate surface, a fifth portion disposed in the substrate portion and extending along the second trench, a sixth portion extending underneath the second trench, and a seventh portion extending from the second region and along the second trench;

a pair of electrically conductive floating gates each having at least a lower portion thereof disposed in one of the first and second trenches; and

an electrically conductive control gate disposed over and insulated from the channel region fourth portion.

51. The device of claim 50, wherein:

the first floating gate is disposed adjacent to and insulated from the first, second and third portions of the channel region for controlling a conductivity thereof; and

the second floating gate is disposed adjacent to and insulated from the fifth, sixth and seventh portions of the channel region for controlling a conductivity thereof.

52. The device of claim 50, wherein the channel region first, third, fifth and seventh portions are generally perpendicular to the substrate surface, and the channel region second, fourth and sixth portions are generally parallel to the substrate surface.

53. The device of claim 50, wherein the floating gates extend deeper into the substrate than do the first and second regions.

54. The device of claim 50, further comprising:

a pair of conductive erase gates that are insulated from the floating gates and the control gate, wherein each of the floating gates has an edge that faces one of the erase gates and is insulated therefrom with insulation material having a thickness that permits tunneling of charges from the edge to the erase gate.